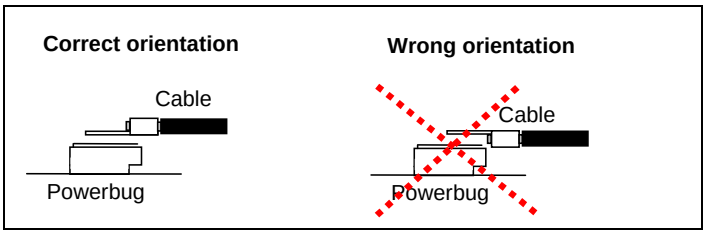
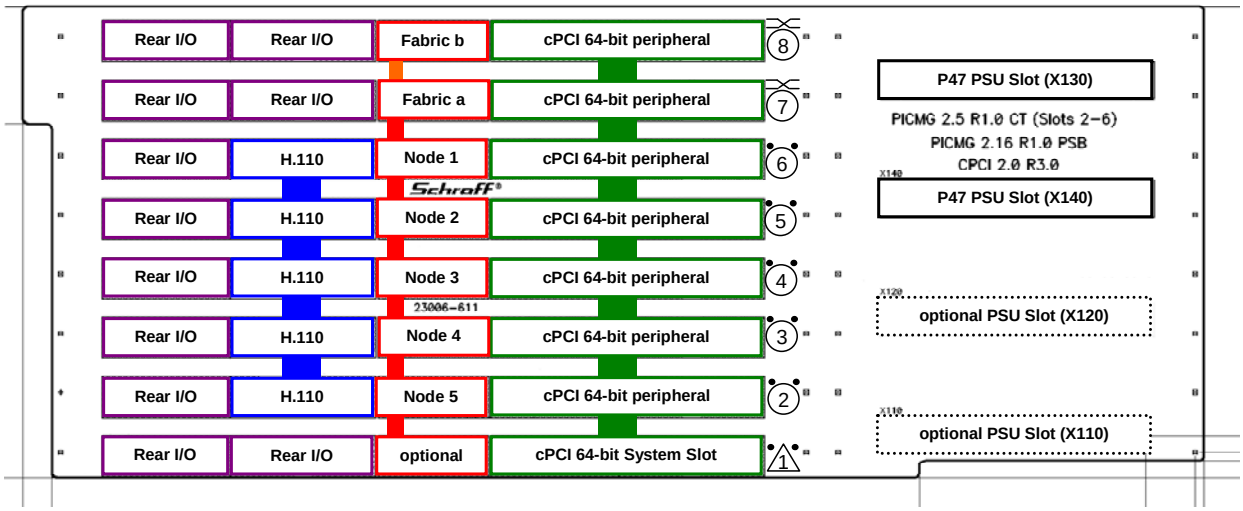
puAssembly Instructions & general Information

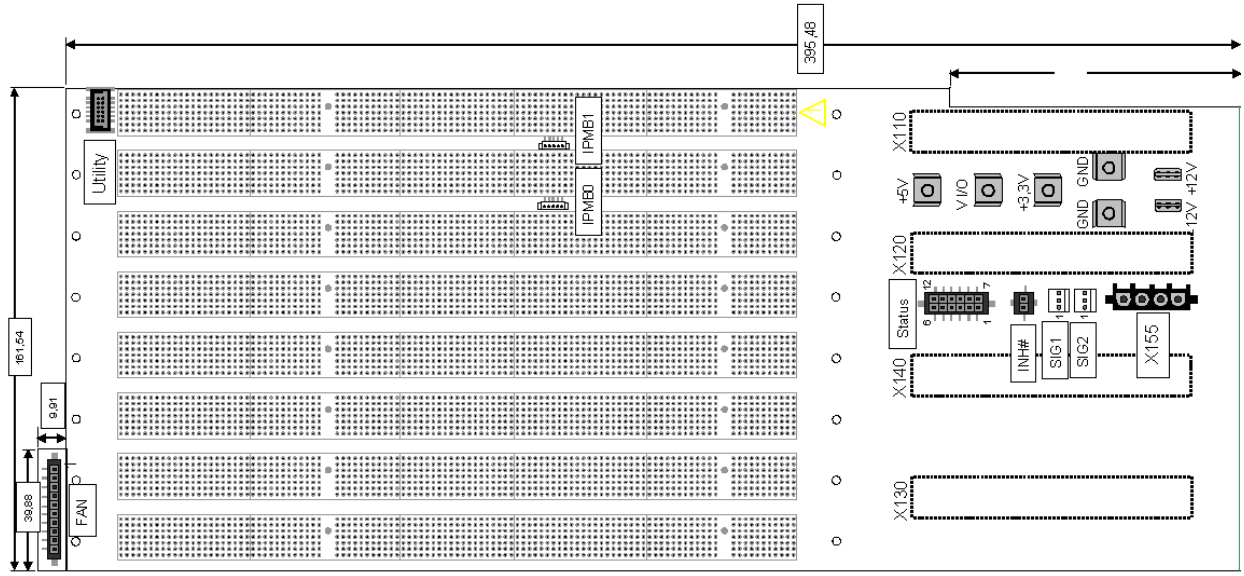
1. **Mechanical Mounting:** Attach the backplane through the mounting holes in at least every second connector position at top and bottom of the CPCI and power slots slots using M2,5 screws and isolating washers.
2. **VI/O:** Check VI/O coding and VI/O (power) bridge, default assembly is +5V (blue key at connector P1). If VI/O shall be set to 3,3V, use conversion kit (order# 21101-658, including keys and tool) to change keys and move the bridge between the power slots.
3. **Geographical Addressing** (GA) is set by default to start from number one from bottom position within the chassis.A change of geographical addresses can be made. Cut copper links in between SMD pads to open, and zero Ohm resistors to close. Package size shall be 0603. Position is labelled "nGA[x]" where "n" stands for slot# , and "x" for address#, see drawing #1.
4. **Hot Swap:** Schroff CPCI backplanes fulfil the requirements for Basic Hot Swap of the Hot Swap Specification PICMG 2.1 R2.0. The signal BD_SEL# is tied to GND by a removable copper link. It can be replaced by a resistor-capacitor combination, both of package size 0603. Position is labelled "nB" where "n" stands for slot# , see drawing.
5. **Dimensions** 405.45 x 161.56mm
6. **Power input:** Power input is realized with P47 connectors below the CPCI slots. 2 CPCI power input slots (3U, 8HP) are equipped with the P47 connectors. 2 additional power slots can be equipped on request. The AC power is brought to the P47 connectors by “feed through” contacts.
7. **Assembling of Power Cables (optional power output using the power bugs):** M4 cable lugs should be used to connect the power output cables to the powerbugs on the backplane. Maximum 2 cables are allowed per powerbug. Please assemble the cable lugs with the flat side to the power bug to ensure the correct isolation distance between unisolated part of the power cable and unisolated parts of the backplane.



8. **CPSB Links / H.110 Bus**
   - 2 Fabric Slots including optional Link between both
   - 5 Node Slots, Node capability of the CPCI system slot can be implemented on request
   - 2 PSU Slots acc. to PICMG 2.11 (2x 3U PSU’s)
   - Fabric Slots are placed right of the Node Slots
   - CompactPCI bus (PICMG2.0 R.3.0) is implemented at all 8 Slots, 64-bit, System slot left
   - Computer Telephony Bus (H.110) is implemented on the P4 area, Slot 2 to 6
   - Applicable Specifications:
     - PICMG 2.16 R1.0 Packed Switched Backplane
     - PICMG 2.5 R1.0 Computer Telephony Specification
     - PICMG 2.0 R3.0 CPCI Core Specification
     - PICMG 2.01 R2.0 Hot Swap
     - PICMG 2.09 R1.0 System Management Bus
     - PICMG 2.10 R1.0 Keying
     - PICMG 2.11 R1.0 Power Interface Specification



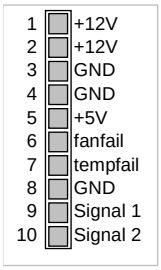
23006-611 Backplane Topology (front view)



23006-611 Backplane (rear view)

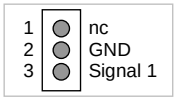
Connectors:

Fan

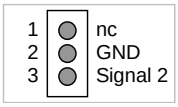


INH#

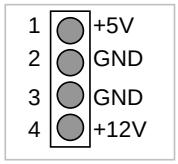
Sig1



Sig2



X155



P47 (X110 – X140)

Pin#	Signal Name	Description
1	V1	V1 Output (+5V)
2	V1	V1 Output (+5V)
3	V1	V1 Output (+5V)
4	V1	V1 Output (+5V)
5	RTN	V1 and V2 Return (GND)
5	RTN	V1 and V2 Return (GND)
7	RTN	V1 and V2 Return (GND)
8	RTN	V1 and V2 Return (GND)
9	RTN	V1 and V2 Return (GND)
10	RTN	V1 and V2 Return (GND)
11	RTN	V1 and V2 Return (GND)
12	RTN	V1 and V2 Return (GND)
13	V2	V2 Output (3,3V)
14	V2	V2 Output (3,3V)
15	V2	V2 Output (3,3V)
16	V2	V2 Output (3,3V)
17	V2	V2 Output (3,3V)
18	V2	V2 Output (3,3V)
19	RTN	V3 Return (GND)
20	V3	V3 Output (+12V)
21	V4	V4 Output (-12V)
22	RTN	Signal Return (GND)
23	RESERVED	Reserved
24	RTN V4	V4 Return (GND)
25	GA0	Geographic Address Bit 0
26	RESERVED	Reserved
27	EN#	Enable (set to GND)
28	GA1	Geographic Address Bit 1
29	V1ADJ	V1 Adjust
30	V1 SENSE	V1 Remote Sense
31	GA2	Geographic Address Bit 2
32	V2ADJ	V2 Adjust
33	V2 SENSE	V2 Remote Sense
34	S RTN	Sense Return
35	V1 SHARE	V1 Current Share
36	V3 SENSE	V3 Remote Sense
37	IPMB_SCL	System Management Bus
38	DEG#	Degrade Signal
39	INH#	Inhibit
40	IPMB_SDA	System Management Bus
41	V2 SHARE	V2 Current Share
42	FAL#	Fail Signal
43	IPMB_PWR	System Management Bus
44	V3 SHARE	V3 Current Share
45	CGND	Chassis Ground (safety ground)
46	ACN/+DC IN	AC Input – Neutral; +DC Input
47	ACL/-DC	IN AC Input – Line; =-DC Input

Status